In the Claims:

1. (Currently Amended) A semiconductor structure comprising:

a semiconductor substrate that includes a first semiconductor material and a second semiconductor material comprising silicon (Si), germanium (Ge), and carbon (C), wherein the first semiconductor material has a lattice constant that is different from a lattice constant of the second semiconductor material;

a first transistor formed in the semiconductor substrate, the first transistor having first source and drain regions formed in the substrate oppositely adjacent a first channel region, wherein a first gate dielectric overlies the first channel region and a first gate electrode overlies the first gate dielectric, and wherein the first channel region is formed in the first semiconductor material and at least a portion of the first source and drain regions are formed in the second semiconductor material, and wherein the second semiconductor material is only substantially outside a region underlying the first gate electrode;

a silicide region on at least a portion of the second semiconductor material, and

a second transistor formed in the semiconductor substrate, having a conductivity type different than a conductivity type of the first transistor, the second transistor having second source and drain regions in the substrate oppositely adjacent a second channel region, wherein a second gate dielectric covers the second channel region and a second gate electrode covers the second gate dielectric.

2. (Original) The structure of claim 1 wherein the first transistor is coupled to the second transistor to form an inverter.

3. (Original) The structure of claim 1 wherein the first transistor is coupled to the second transistor as part of a NOR circuit.

4. (Original) The structure of claim 1 wherein the first transistor is coupled to the second transistor as part of a NAND circuit.

5. (Original) The structure of claim 1 wherein the first transistor is coupled to the second transistor as part of an XOR circuit.

6. (Original) The structure of claim 1 wherein the first and second gate dielectrics are formed from a high-k dielectric.

7. (Original) The structure of claim 1 wherein the first and second gate electrodes comprise a metal material.

8. (Original) The structure of claim 1 wherein the lattice constant of the second semiconductor material is larger than the lattice constant of the first semiconductor material.

9. (Original) The structure of claim 8 wherein the first transistor is a PMOS transistor.

10.-11. (Cancelled)

12. (Currently Amended) The structure of claim [[10]]1 wherein ~~the concentration of Ge is~~ Ge has a concentration of greater than 10 percent.

13. (Cancelled)

14. (Currently Amended) The structure of claim [[13]]1 wherein the first transistor is an NMOS transistor.

15. (Cancelled)

16. (Currently Amended) The structure of claim [[15]]14 wherein the second semiconductor material comprises silicon, germanium, and carbon.

17. (Currently amended) The structure of claim [[15]]14 wherein ~~the concentration of carbon is~~ carbon has a concentration in the range of 0.01 percent to 0.04 percent.

18.-21. (Canceled)

22. (Original) The structure of claim 1 wherein the first transistor comprises a PMOS transistor and the second transistor comprises an NMOS transistor and wherein the ratio of a width of the gate of the PMOS transistor to a width of the gate of the NMOS transistor is approximately equal to the square root of a ratio of electron mobility to the hole mobility in the channel region.

23. (Original) The structure of claim 1 wherein the first transistor comprises a PMOS transistor and the second transistor comprises an NMOS transistor and wherein the ratio of a width of the gate of the PMOS transistor to a width of the gate of the NMOS transistor is approximately equal to the ratio of electron mobility to hole mobility in the channel region.

24. (Cancelled)

25. (Original) The structure of claim 1 wherein the distance between a junction between the first semiconductor material and the second semiconductor material and the gate dielectric edge is less than 700 angstroms.

26. (Currently Amended) An inverter comprising:

a transistor formed in the semiconductor substrate, the transistor having a source region and a drain region formed in a semiconductor substrate oppositely adjacent a channel region, wherein the channel is formed in a first semiconductor material and at least a portion of the source region and the drain region is formed in a second semiconductor material comprising silicon (Si), germanium (Ge), and carbon (C), the first semiconductor material being different than the second semiconductor material, and wherein a gate dielectric overlies the channel region and a gate electrode overlies the gate dielectric, and wherein a region underlying the gate electrode is substantially free of the first semiconductor material;

a silicide region on at least a portion of the second semiconductor material;

a load element formed in the semiconductor substrate, the load element coupled between the drain region and a first supply voltage node; and

a second supply voltage node coupled to the source region.

27. (Original) The inverter of claim 26 wherein the load element comprises a resistor and the transistor comprises an NMOS transistor.

28. (Original) The inverter of claim 26 wherein the load element comprises a resistor and the transistor comprises a PMOS transistor.

29. (Original) The inverter of claim 26 wherein the load element comprises a transistor.

30. (Original) The inverter of claim 29 wherein the load element comprises a strained transistor.

31. (Original) The inverter of claim 26 wherein the transistor includes a gate dielectric overlying the channel region, the gate dielectric being formed from a high-k dielectric.

32. (Original) The inverter of claim 31 wherein the transistor includes a gate electrode overlying the gate dielectric, the gate electrode comprising a metal material.

33. (Original) The inverter of claim 26 wherein a lattice constant of the second semiconductor material is larger than a lattice constant of the first semiconductor material.

34. (Original) The inverter of claim 33 wherein the transistor is a PMOS transistor.

35. (Cancelled)

36. (Currently Amended) The inverter of claim [[35]]26 wherein the concentration of Ge is greater than 10 percent.

37. (Original) The inverter of claim 26 wherein the lattice constant of the second semiconductor material is smaller than the lattice constant of the first semiconductor material.

38. (Original) The inverter of claim 37 wherein the transistor is an NMOS transistor.

39. (Cancelled)

40. (Currently Amended) The inverter of claim [[39]]26 wherein the concentration of carbon is in the range of 0.01 percent to 0.04 percent.

41. (Currently Amended) The inverter of claim 26 wherein the ~~first and second~~ source and drain regions and the gate electrode ~~electrodes of the first and second transistors~~ of the transistor each include a silicided portion.

42. (Original) The inverter of claim 26 wherein the first semiconductor material consists essentially of silicon.

43.-44. (Cancelled)

45. (Original) The inverter of claim 26 wherein the semiconductor substrate further comprises an insulator layer underlying the first semiconductor material.

46. (Original) The inverter of claim 26 and further comprising a conductive material formed over the source region and the drain region.

47. (Currently Amended) The inverter of claim 46 wherein the conductive material at least one material selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide, tantalum silicide, erbium silicide, iridium silicide, cobalt germanosilicide, nickel germanosilicide, cobalt carbon-silicide, and nickel carbon-silicide.

48. (Original) The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrodc overlying the gate dielectric, the gate electrode being formed from a semiconductor.

49. (Original) The inverter of claim 48 wherein the gate electrode is formed from polycrystalline silicon.

50. (Original) The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, the gate electrode being formed from a metal.

51. (Original) The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, the gate electrode being formed from a metal silicide.

52. (Original) The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, the gate electrode being formed from a metal nitride.

53. (Original) The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrodc overlying the gate dielectric, wherein the gate dielectric comprises at least one material selected from the group consisting of silicon oxide, silicon oxynitride, and silicon nitride.

54. (Original) The inverter of claim 26 wherein the transistor comprises a gate dielectric overlying the channel region and a gate electrode overlying the gate dielectric, wherein the gate dielectric comprises a high k dielectric.

55. (Original) The inverter of claim 54 wherein the gate dielectric comprises at least one material selected from the group consisting of hafnium oxide, aluminum oxide, and zirconium oxide, and combinations thereof.

56.-77. (Canceled)

78. (Currently Amended) A semiconductor structure comprising:

a semiconductor substrate that includes a first semiconductor material, a second semiconductor material comprising silicon (Si), germanium (Ge), and carbon (C), and a third semiconductor material, wherein the lattice constant of the second semiconductor material is larger than lattice constant of the first semiconductor material and the lattice constant of the third material is smaller than the lattice constant of the first material;

a first transistor formed in the semiconductor substrate, the first transistor having first source and drain regions formed in the substrate oppositely adjacent a first channel region, wherein a first gate dielectric overlies the first channel region and a first gate electrode overlies the first gate dielectric, and wherein the first channel region is formed in the first semiconductor material and at least a portion of the first source and drain regions are formed in the second semiconductor material;

a silicide region on at least a portion of the second semiconductor material;

a second transistor formed in the semiconductor substrate, having a conductivity type

different than the first transistor, the second transistor having second source and drain regions in the substrate oppositely adjacent a second channel region, wherein a second gate dielectric covers the second channel region and a second gate electrode covers the second gate dielectric; and

wherein at least a portion of the second source and drain regions are formed in the third semiconductor material, and wherein the second semiconductor material is only substantially outside a region underlying the first gate electrode.

79. (Previously presented) The structure of claim 78 wherein the first transistor is a PMOS and the second transistor is an NMOS.

80. (Previously presented) The structure of claim 78 wherein the third semiconductor material comprises silicon, germanium and carbon.